

**CPU CORE**  
SENTECH  
SC451  
Page: 25

**+3VPCU**  
**+3V\_S5/+3VSUS**  
**+3V**  
**+5VSUS/+5V**  
**10V/15V**  
**+1.8V\_S5**  
MAXIM  
MAX8744ETJ+  
Page: 26

**+1.8VSUS/+1.8V**  
**+1.2V**  
MAXIM  
MAX8743EEI  
Page: 27

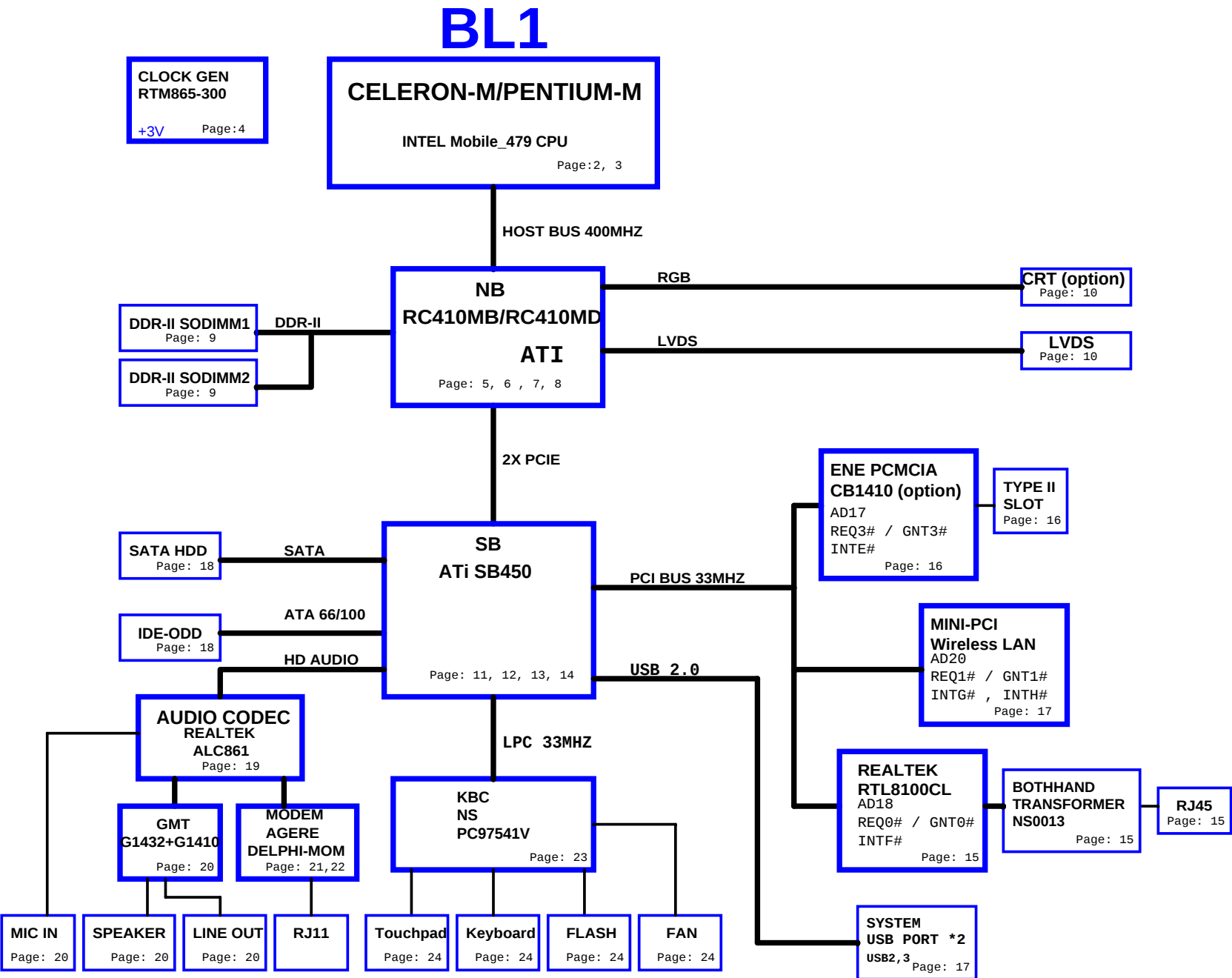
**+1.05V**  
SENTECH  
SC4215\*2  
Page: 29

**+0.9VSUS**  
**+0.9V**  
GMT  
G2996  
Page: 26, 29

**BATTERY CHARGER**  
MAXIM  
MAX8724  
Page: 28

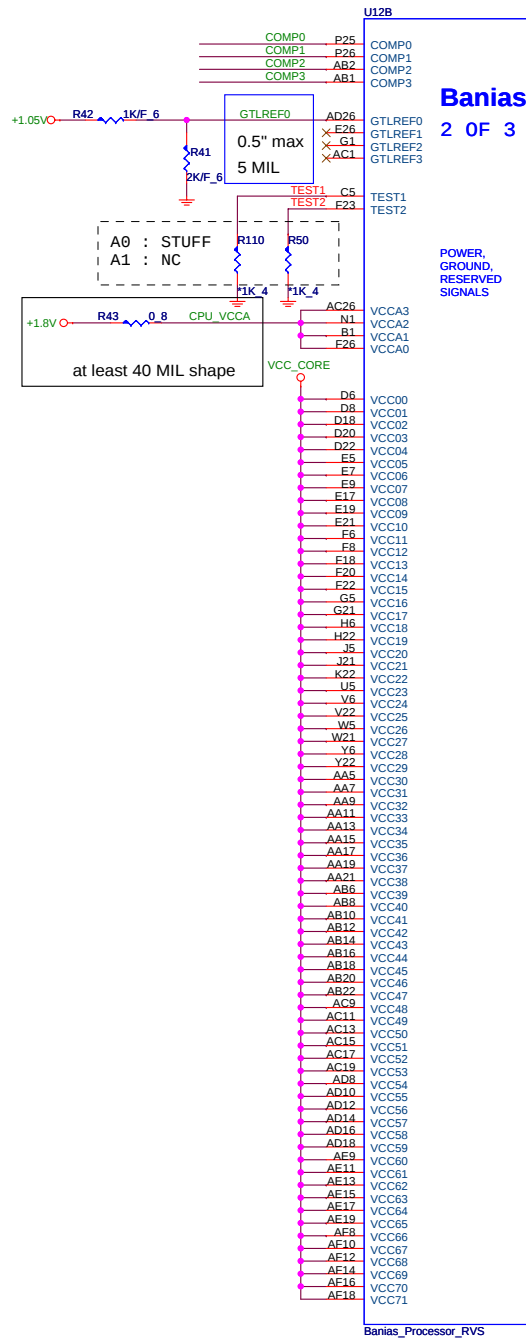
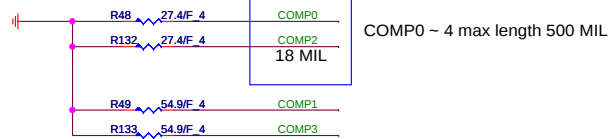
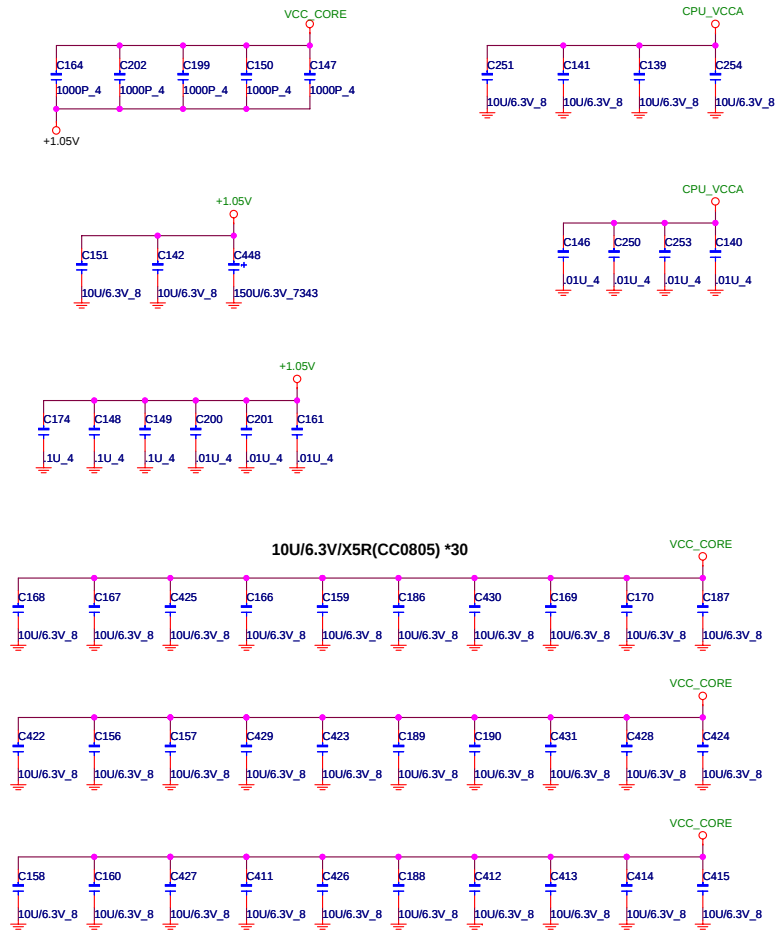
**Power State Table**

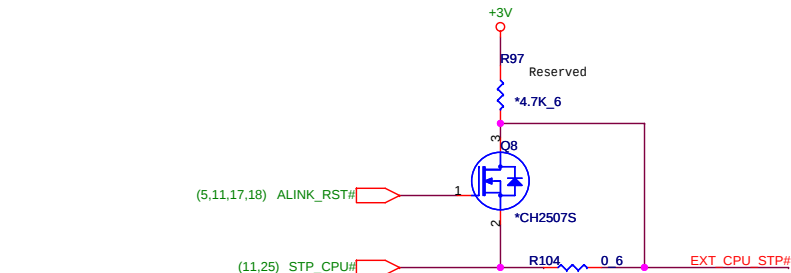
| Power Name | Control Signal | Power State | Power Source |
|------------|----------------|-------------|--------------|
| VCC_CORE   | VRON           | S0          | VIN          |
| +3VPCU     | N7A            | ALWAYS      | VIN          |
| +3V_S5     | S5_ON          | S0-S5       | +3VPCU       |
| +3VSUS     | SUSON          | S0-S3       | +3VPCU       |
| +3V        | MAINON         | S0          | +3VPCU       |
| +5VPCU     | N7A            | ALWAYS      | VIN          |
| +5V_S5     | S5_ON          | S0-S5       | +5VPCU       |
| +5VSUS     | SUSON          | S0-S3       | +5VPCU       |
| +5V        | MAINON         | S0          | +5VPCU       |
| 15V/10V    | N/A            | S0          | +5VPCU       |
| +1.2V      | MAINON         | S0          | VIN          |
| +1.05V     | MAINON         | S0          | +1.8VSUS     |
| +0.9V      | MAINON         | S0          | +1.8VSUS     |
| +1.8V_S5   | S5_ON          | S0-S5       | +3VPCU       |
| +1.8VSUS   | SUSON          | S0-S3       | VIN          |
| +1.8V      | MAINON         | S0          | +1.8VSUS     |



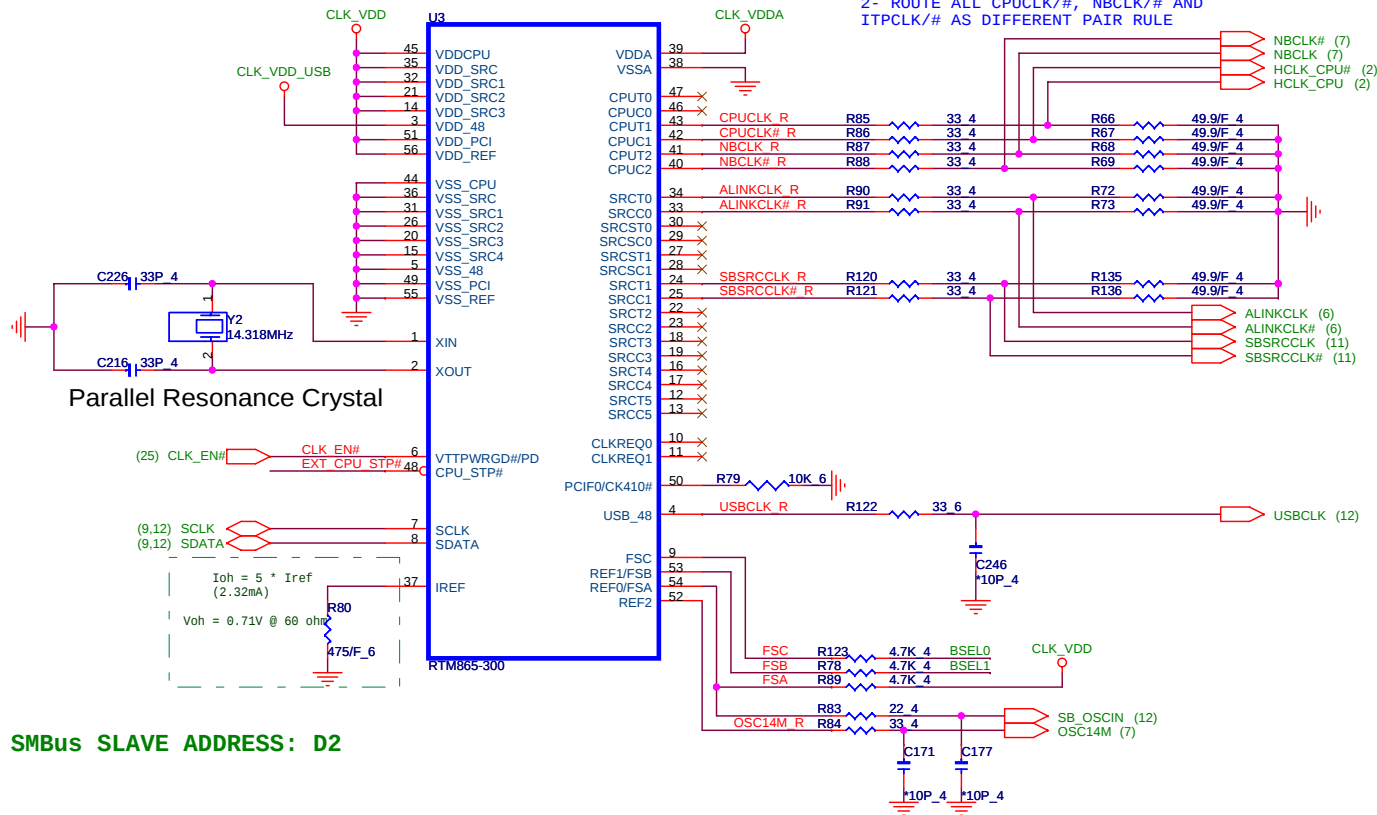


# CPU





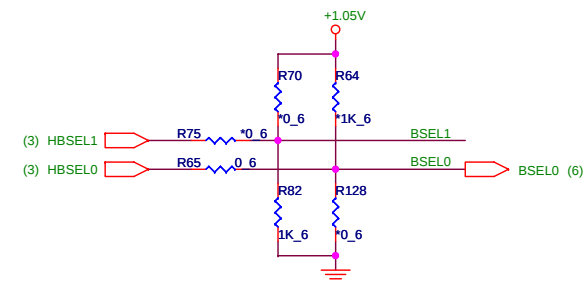
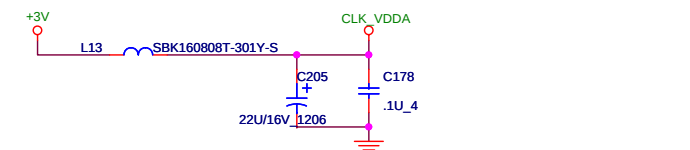
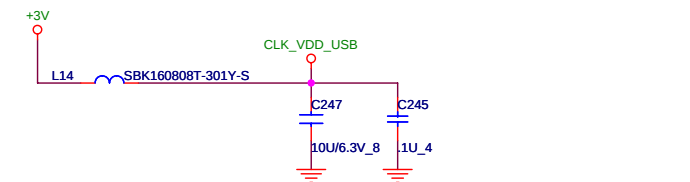
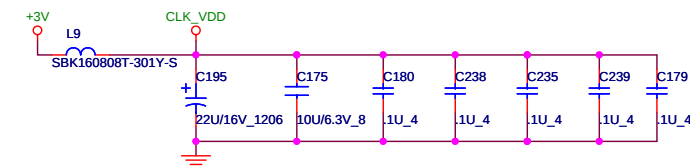
- 1- PLACE ALL THE SERIES TERMINATION RESISTORS AS CLOSE AS CLK GEN AS POSSIBLE
- 2- ROUTE ALL CPUCLK/#, NBCLK/# AND ITPCLK/# AS DIFFERENT PAIR RULE



SMBus SLAVE ADDRESS: D2

CK410 FREQUENCY SELECT TABLE(MHZ)

| FSC<br>BSEL0 | FSB<br>BSEL1 | FSA | CPU<br>MHz |
|--------------|--------------|-----|------------|
| 0            | 0            | 0   | 266.66     |
| 0            | 0            | 1   | 133.33     |
| 0            | 1            | 0   | 200.00     |
| 0            | 1            | 1   | 166.66     |
| 1            | 0            | 0   | 333.33     |
| 1            | 0            | 1   | 100.00     |
| 1            | 1            | 0   | 400.00     |
| 1            | 1            | 1   | Rsvd       |



| HBSEL1 | HBSEL0 |         |
|--------|--------|---------|
| 0      | 0      | 133 MHz |
| 0      | 1      | 100 MHz |

# CLK



PROJECT : BL1  
Quanta Computer Inc.

# CLG

**RC410MB**  
MPVSS need to connect to GND plane immediately through a dedicated VIA

**MEM\_B I/F**

4/04 This pull-up rail is applicable to both DDRII applications and can be at S0 or S3 rail.

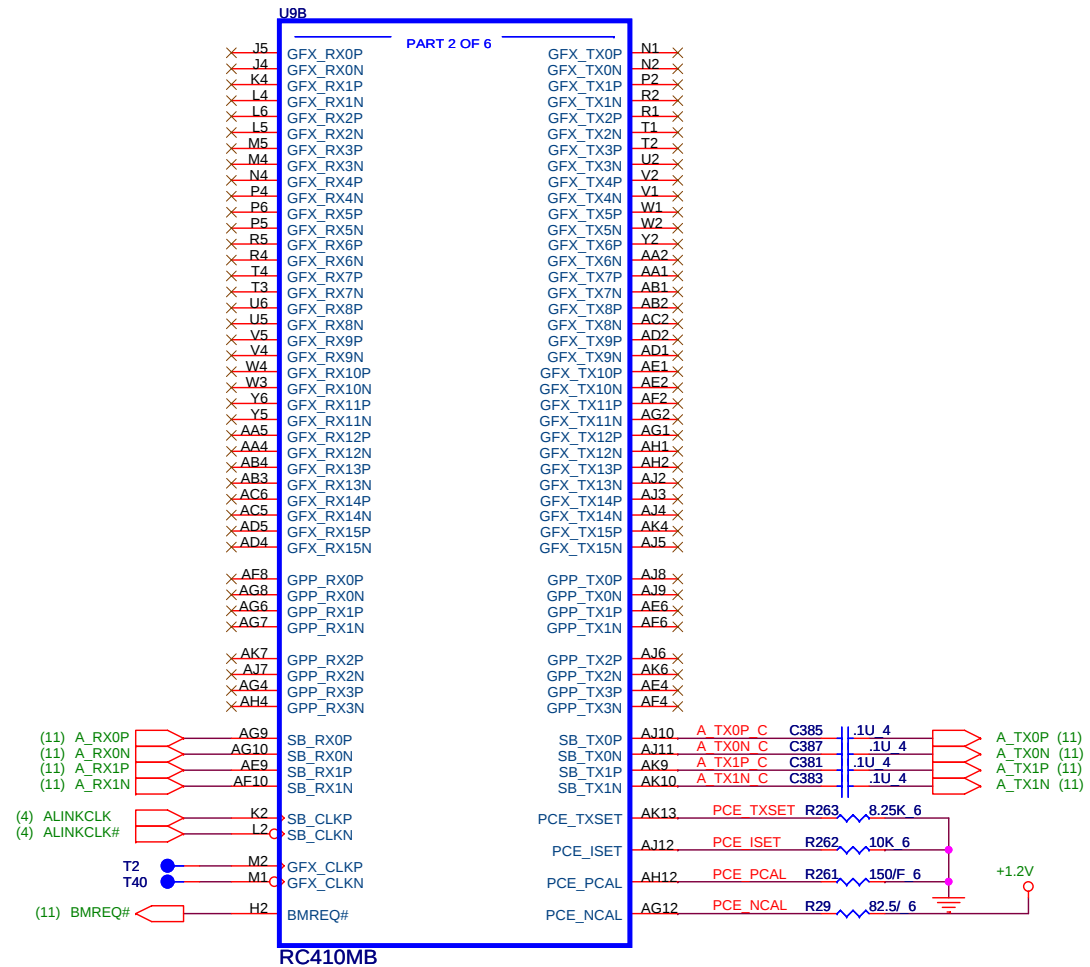
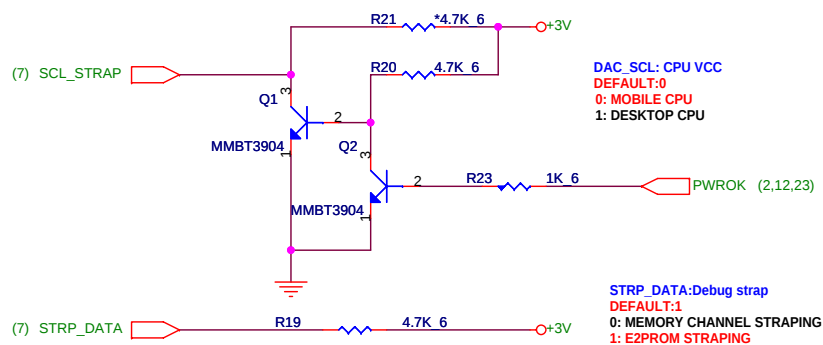
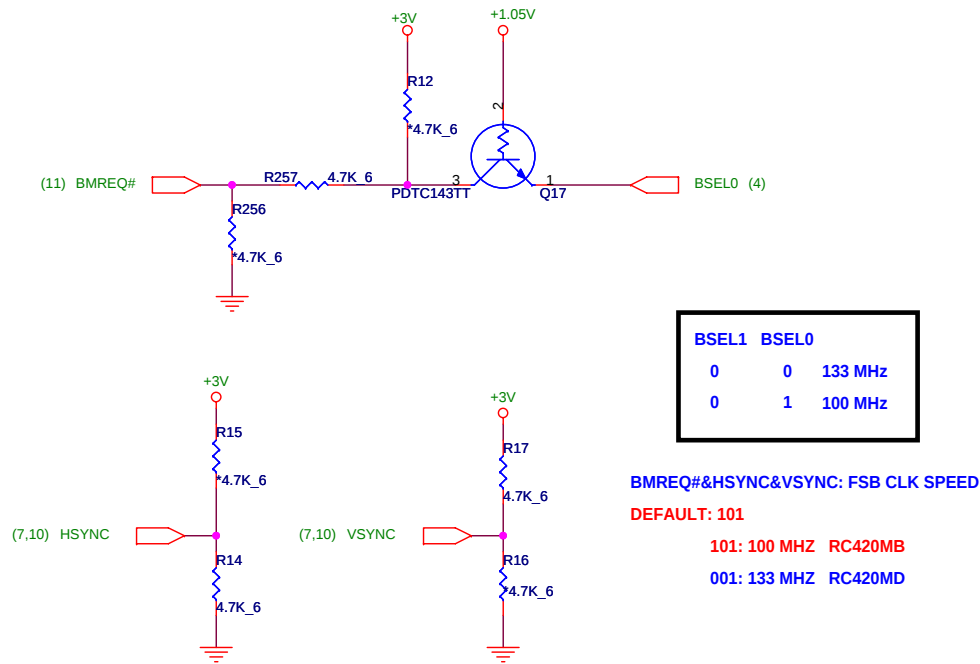
CPVSS need to connect to GND plane immediately through a dedicated VIA



**PROJECT : BL1**  
**Quanta Computer Inc.**

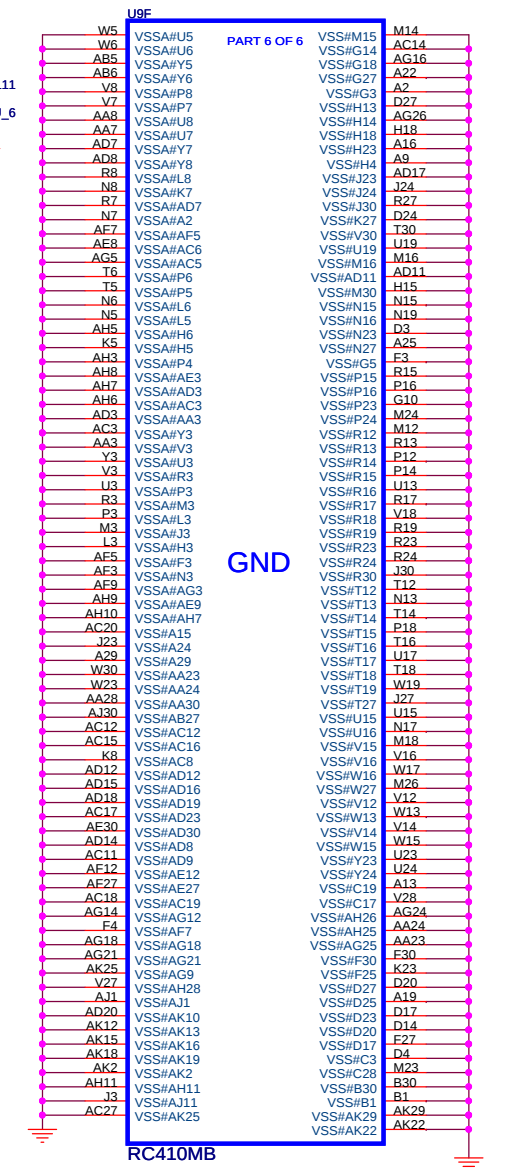
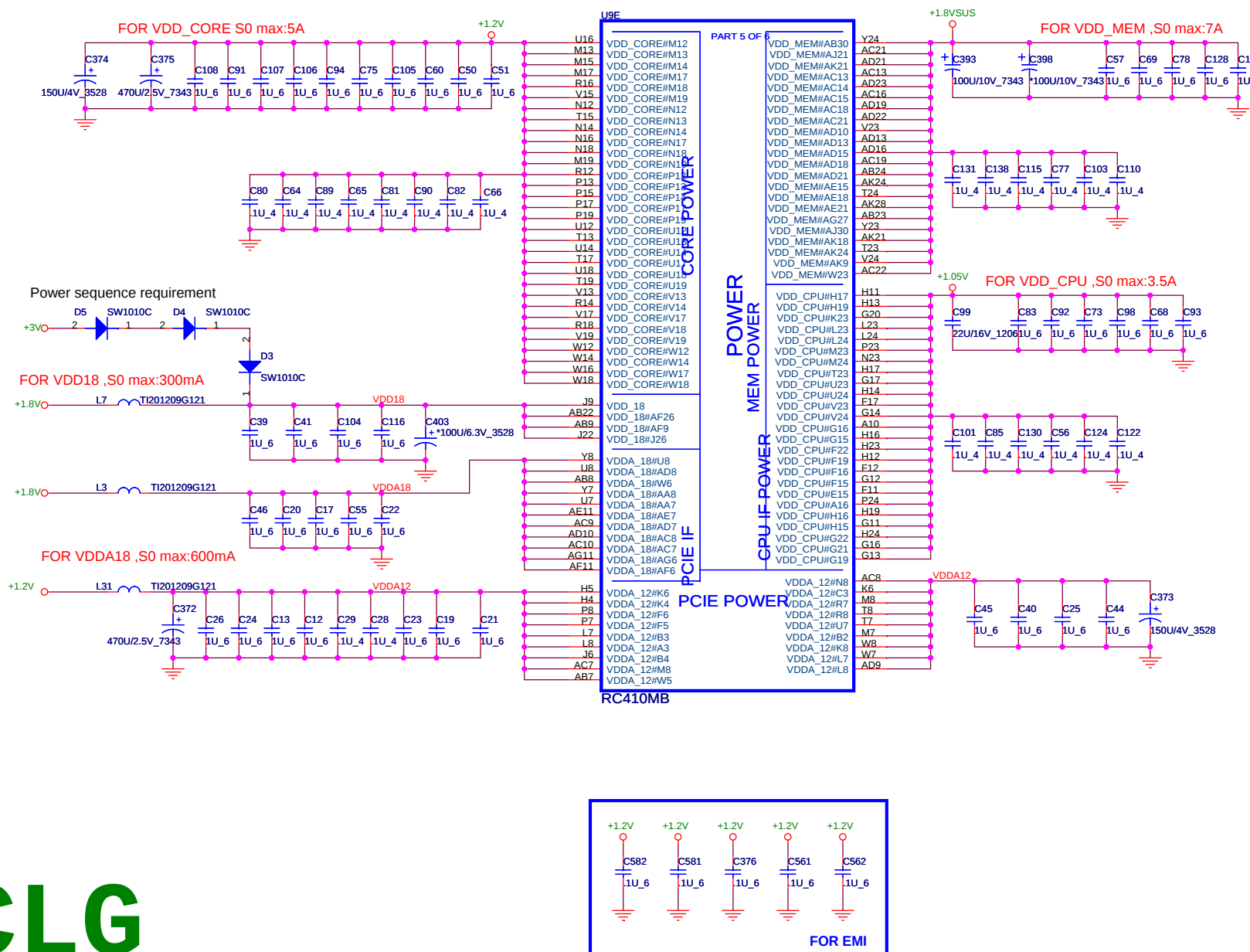
|       |                          |               |
|-------|--------------------------|---------------|
| Size  | Document Number          | Rev           |
|       | <b>RC410MB-AGTL+ I/F</b> | 3A            |
| Date: | Friday, April 28, 2006   | Sheet 5 of 30 |

# NB strapping



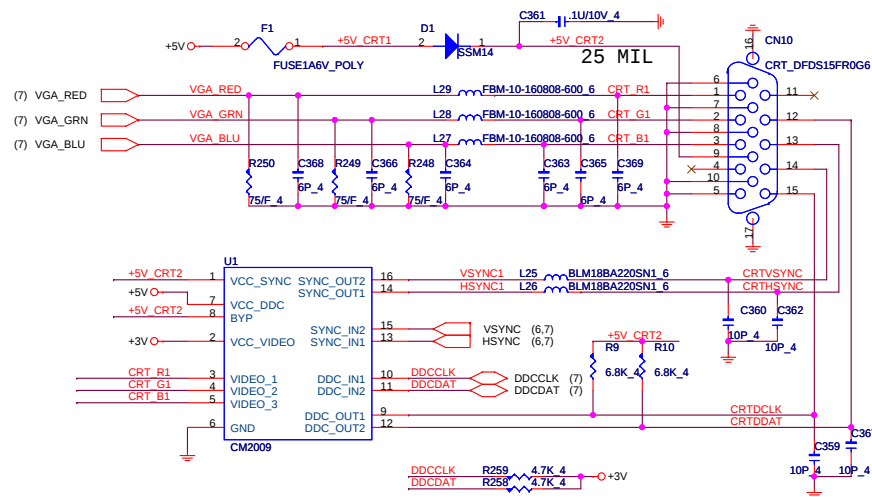


CLG

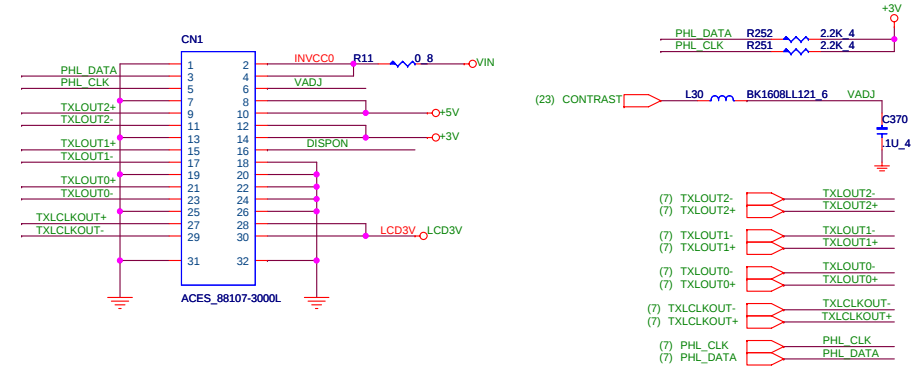




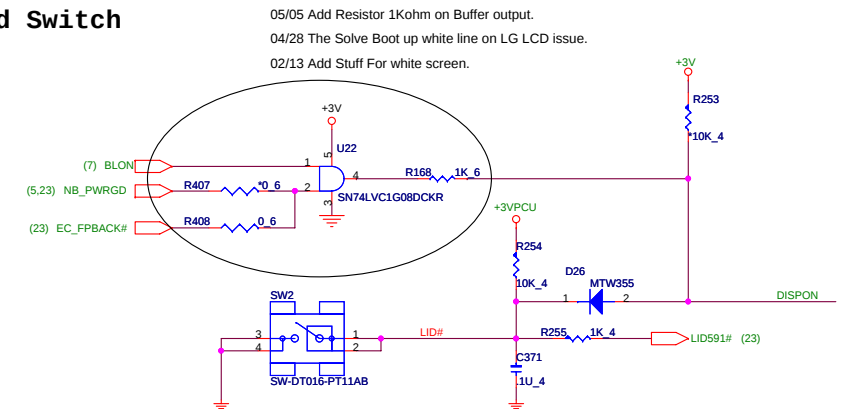
## CRT PORT

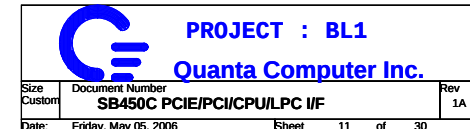


## LCD Connector

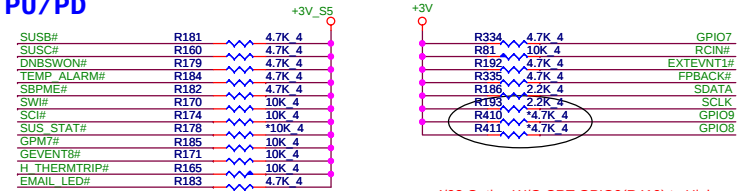


## Lid Switch

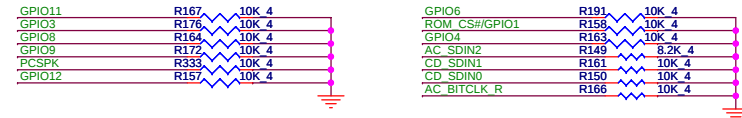




**PU/PD**

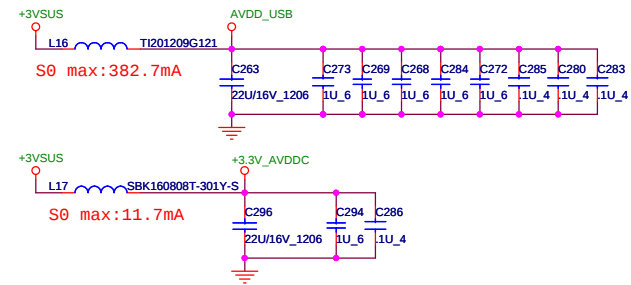
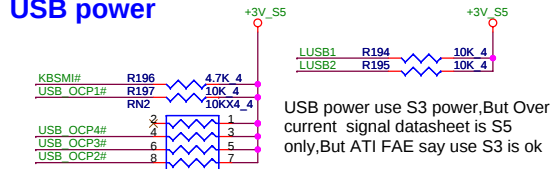


4/02 Option W/O CRT GPIO9(R410) to High.  
4/02 Option(Normal) CRT GPIO9(R172) to Low.

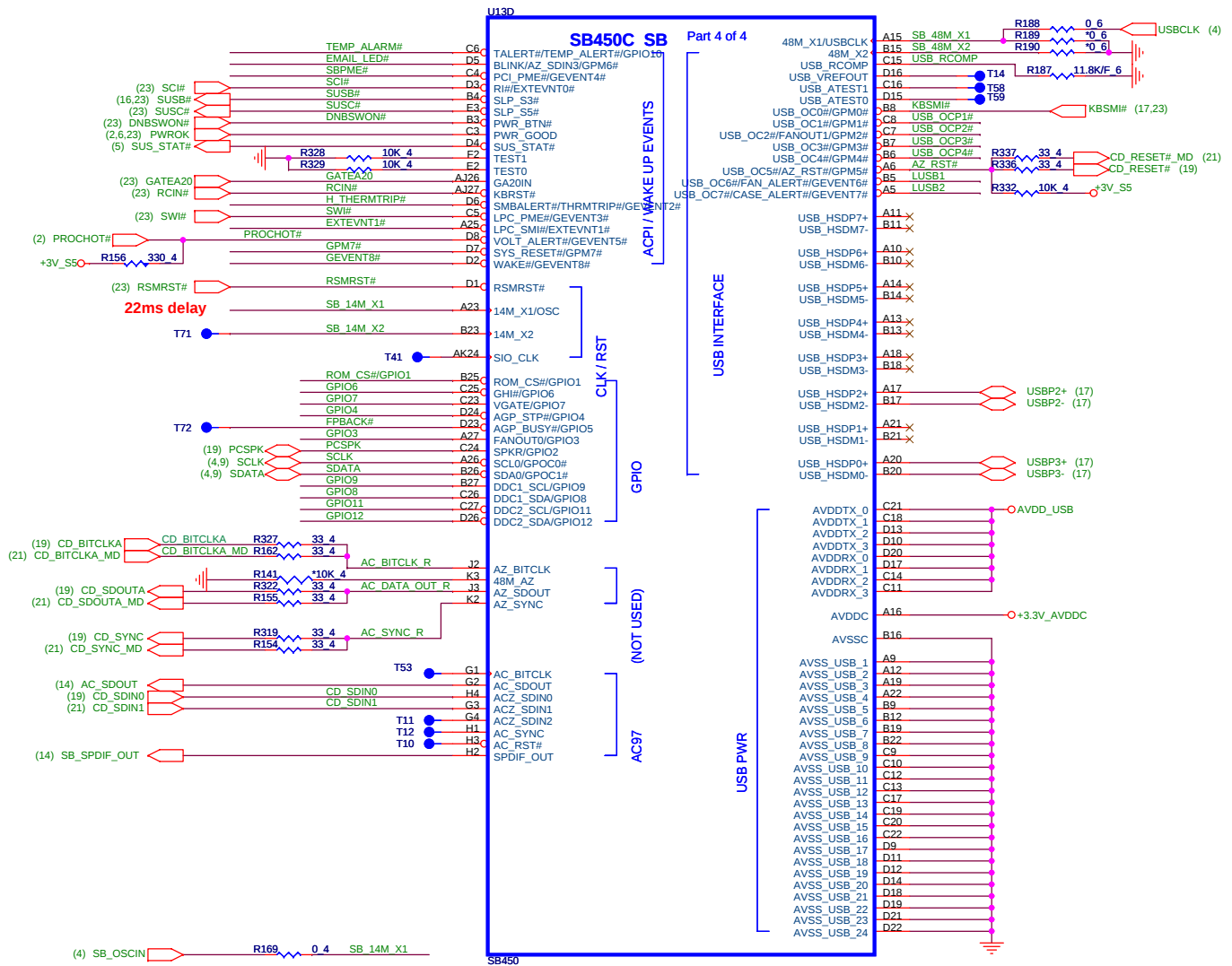


|           |           |           |
|-----------|-----------|-----------|
|           | GPIO9 PIN | GPIO8 PIN |
| CRT       | LOW       |           |
| W/O CRT   | HIGH      |           |
| Modem     |           | LOW       |
| W/O Modem |           | HIGH      |

## USB power



# CLG

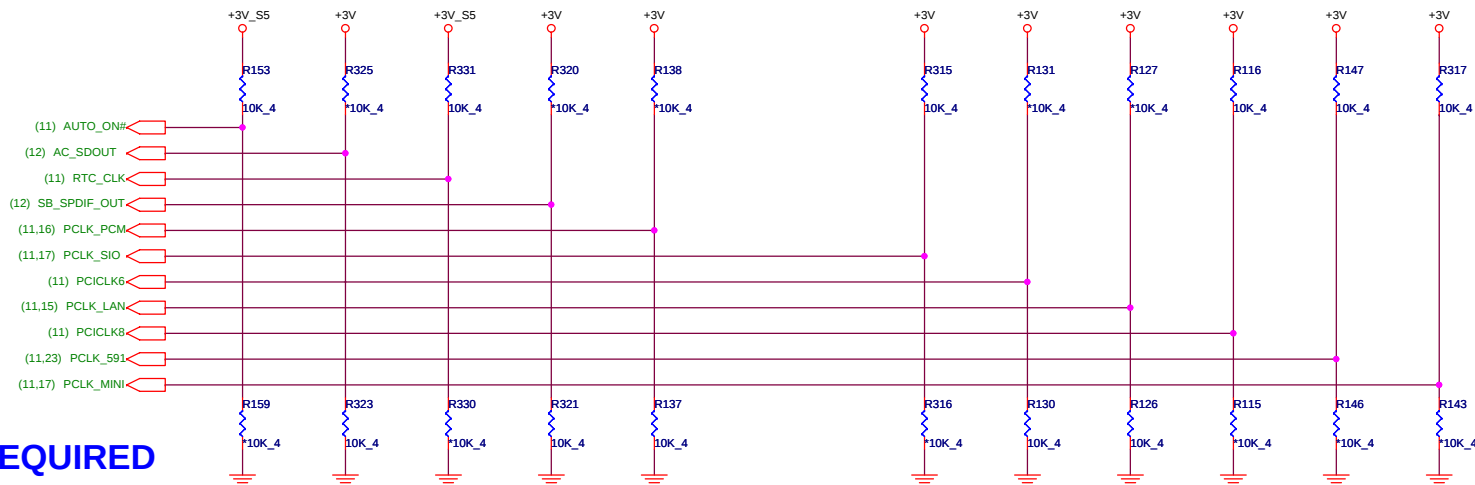


**PROJECT : BL1**  
**Quanta Computer Inc.**

|                            |                                                     |           |
|----------------------------|-----------------------------------------------------|-----------|
| Size Custom                | Document Number<br><b>SB450C ACPI/GPIO/USB/AC97</b> | Rev<br>3A |
| Date: Monday, May 08, 2006 | Sheet 12 of 30                                      |           |



## REQUIRED STRAPS

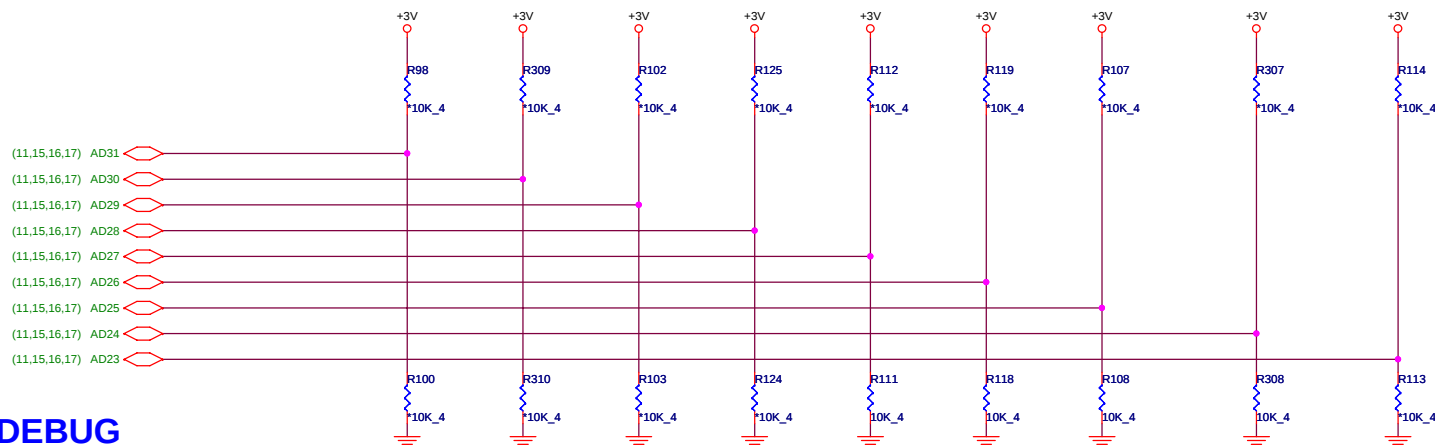


PCI\_CLK4 PCI\_CLK5 PCI\_CLK6 PCI\_CLK7 PCI\_CLK8 PCI\_CLK3 PCI\_CLK2

|           | ACPWRON                      | AC_SDOUT                       | RTC_CLK                                 | SPDIF_OUT                | PCLK_PCM                            | PCLK_SIO                      | PCI_CLK6                    | PCLK_LAN                                                                                                  | PCI_CLK8 | PCLK_591                           | PCLK_MINI*                   |
|-----------|------------------------------|--------------------------------|-----------------------------------------|--------------------------|-------------------------------------|-------------------------------|-----------------------------|-----------------------------------------------------------------------------------------------------------|----------|------------------------------------|------------------------------|
| PULL HIGH | MANUAL PWR ON<br><br>DEFAULT | USE DEBUG STRAPS               | INTERNAL RTC<br><br>DEFAULT             | SIO 24MHz                | 48MHz use Internal PLL              | 14MHz OSC MODE<br><br>DEFAULT | CPU I/F = K8                | H,H = PCI(X BUS) ROM<br>H,L = LPC ROM I (LPC addresses are translated to the top of the 4G address space) |          | USB PHY PWRDOWN DISABLE<br>DEFAULT | 48MHz Crystal Pad<br>DEFAULT |
| PULL LOW  | AUTO PWR ON                  | IGNORE DEBUG STRAPS<br>DEFAULT | EXTERNAL RTC (NOT SUPPORTED W/ IT8712 ) | SIO 48MHz<br><br>DEFAULT | 48MHz use External Clock<br>DEFAULT | 14MHz XTAL MODE               | CPU I/F = P4<br><br>DEFAULT | L,H = LPC ROM II (addresses mapped to below 1M)<br>L,L = FWH ROM                                          |          | USB PHY PWRDOWN ENABLE             | 48MHz OSC/Clock Buffer       |

\*This strap is only required if the strap on PCICLK4 is configured for External Clock.

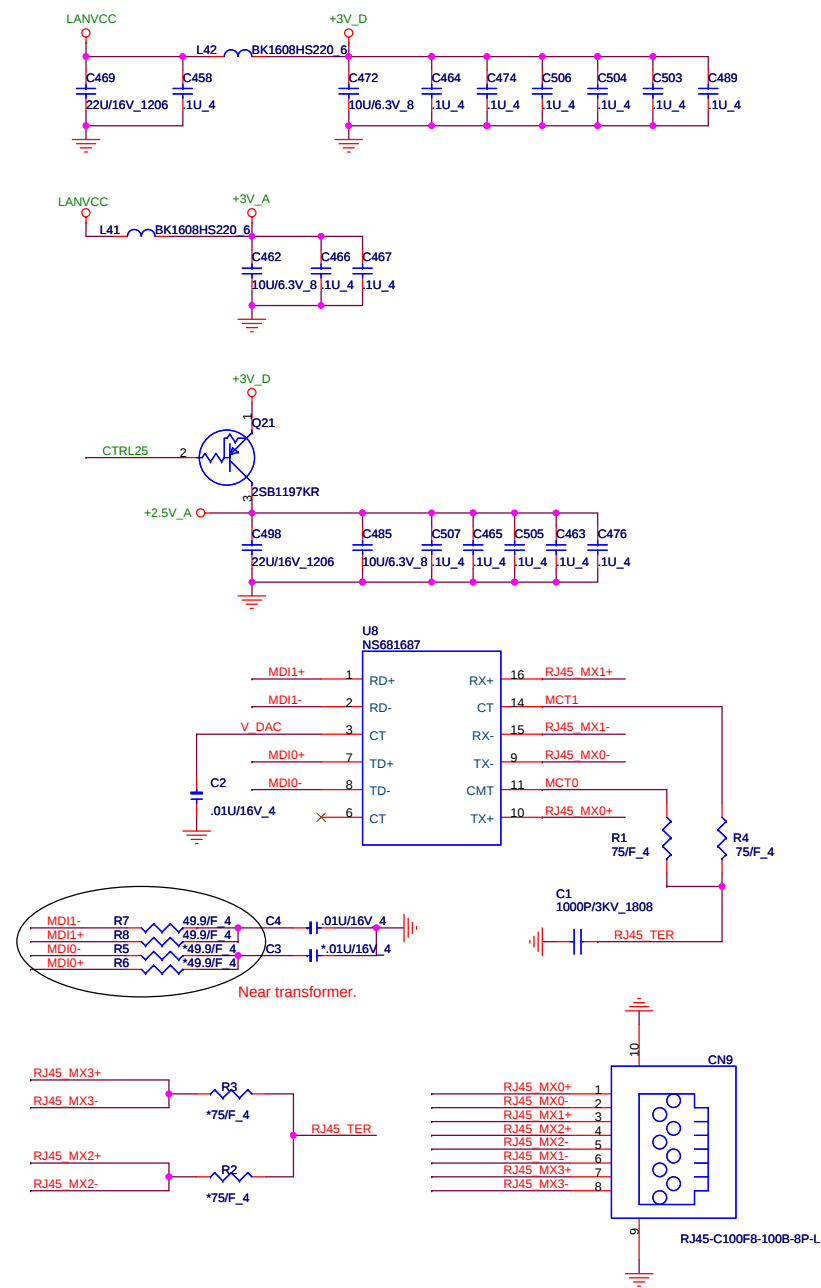
## DEBUG STRAPS



|           | PDACK#                    | PCI_AD31 | PCI_AD30 | PCI_AD29 | PCI_AD28 | PCI_AD27               | PCI_AD26                 | PCI_AD25               | PCI_AD24                           | PCI_AD23 |
|-----------|---------------------------|----------|----------|----------|----------|------------------------|--------------------------|------------------------|------------------------------------|----------|
| PULL HIGH | USE LONG RESET<br>DEFAULT | Reserved | Reserved | Reserved | Reserved | BYPASS PCI PLL         | BYPASS ACPI BCLK         | BYPASS IDE PLL         | USE EEPROM PCIE STRAPS             | Reserved |
| PULL LOW  | USE SHORT RESET           |          |          |          |          | USE PCI PLL<br>DEFAULT | USE ACPI BCLK<br>DEFAULT | USE IDE PLL<br>DEFAULT | USE DEFAULT PCIE STRAPS<br>DEFAULT |          |

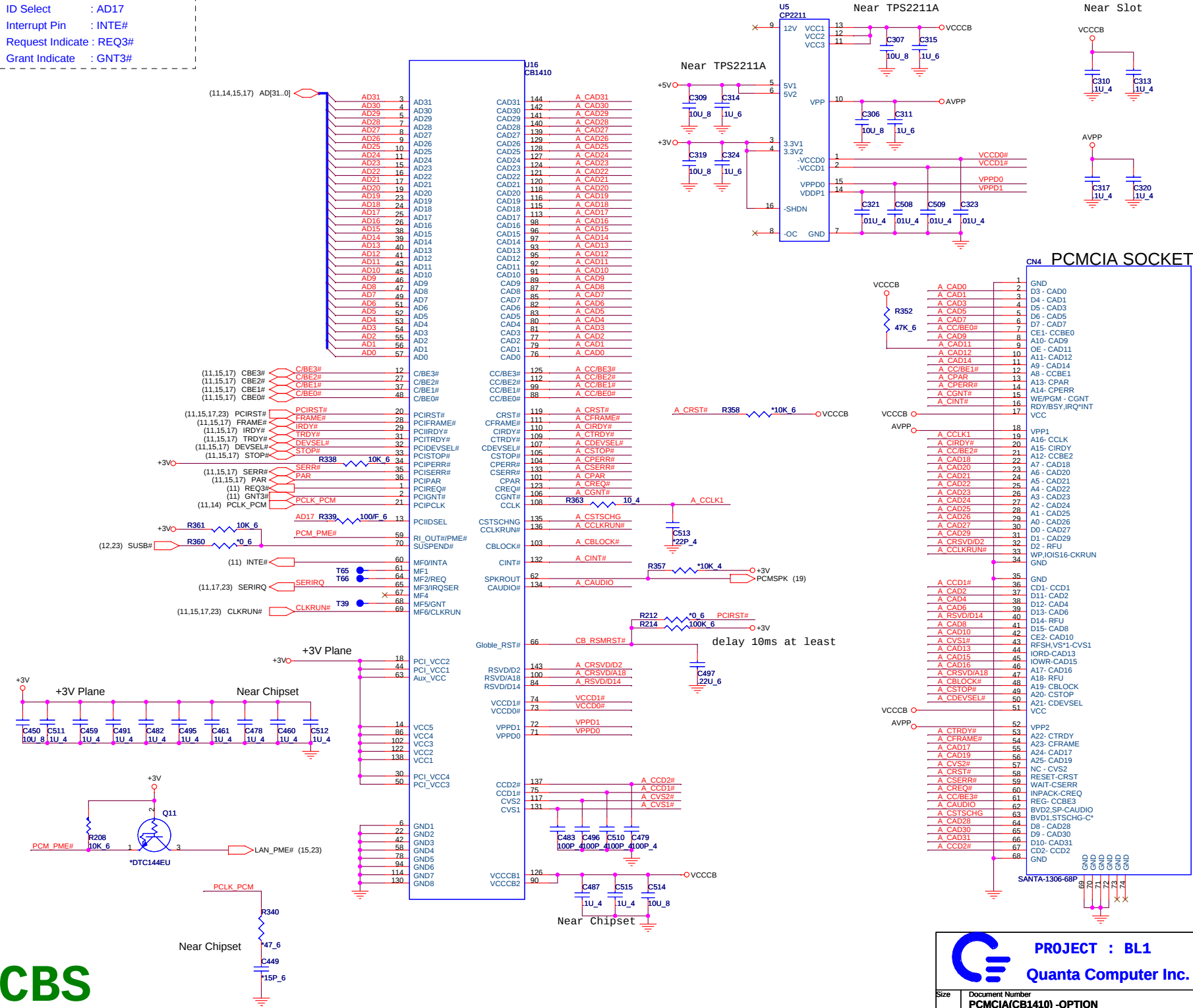
CLG

# LAN



|                                                                                       |                              |           |          |
|---------------------------------------------------------------------------------------|------------------------------|-----------|----------|
|  | <b>PROJECT : BL1</b>         |           |          |
|                                                                                       | <b>Quanta Computer Inc.</b>  |           |          |
| Size                                                                                  | Document Number              | Rev       |          |
|                                                                                       | <b>LAN RTL8110SBL/8100CL</b> | <b>1A</b> |          |
| Date:                                                                                 | Saturday, May 06, 2006       | Sheet     | 15 of 30 |

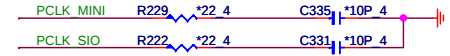
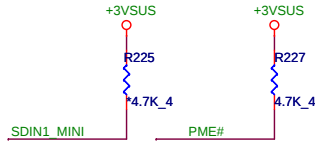
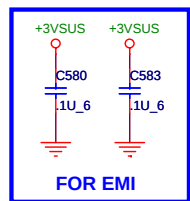
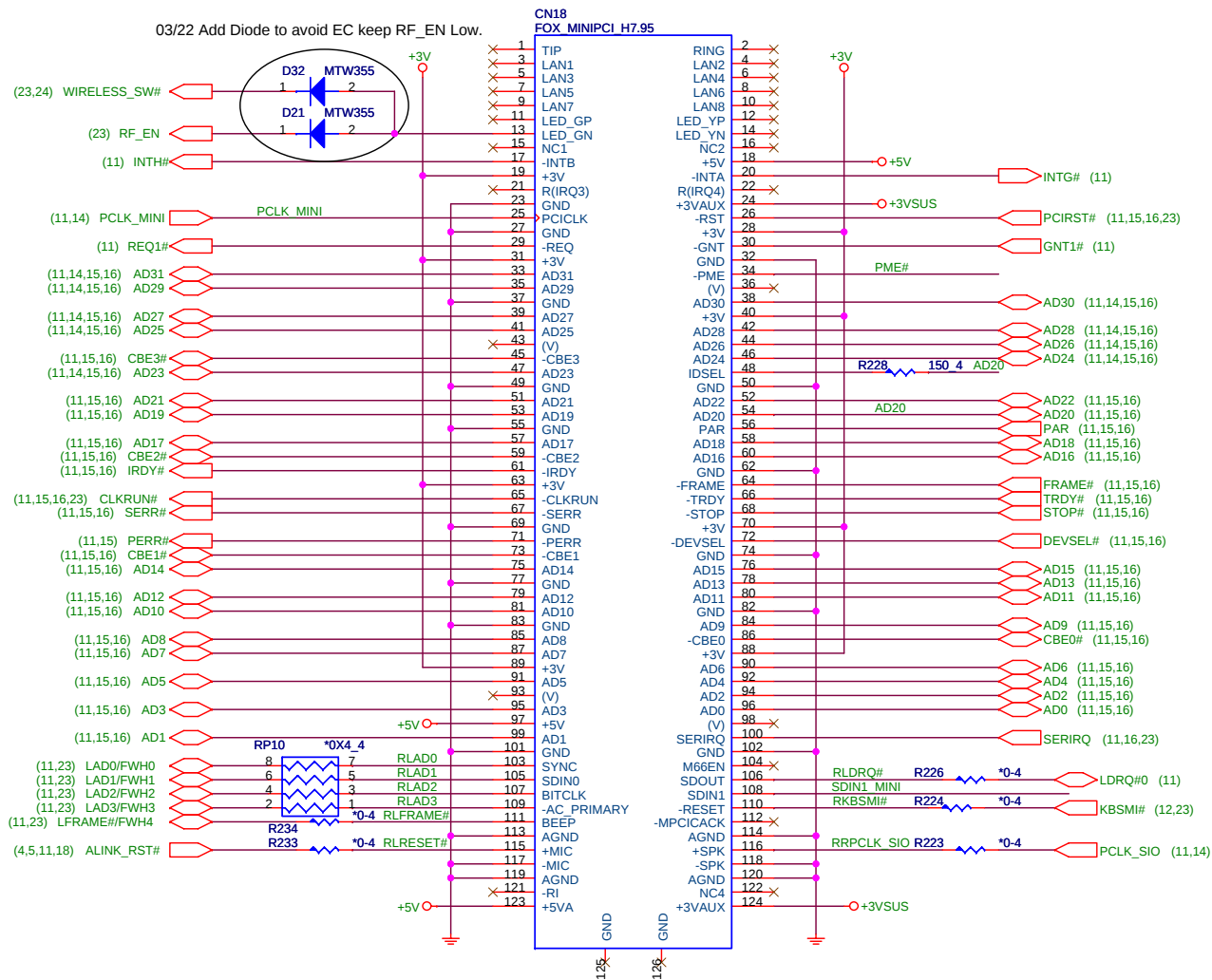
ID Select : AD17  
Interrupt Pin : INTE#  
Request Indicate : REQ3#  
Grant Indicate : GNT3#



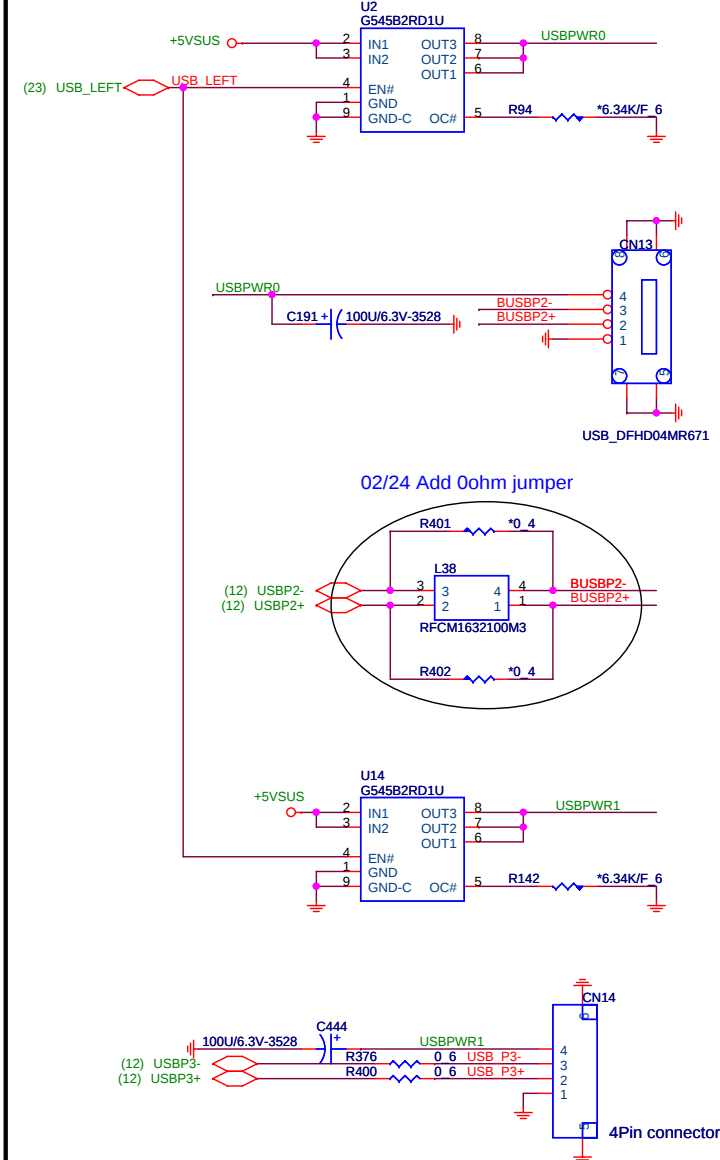
ID Select : AD20  
 Interrupt Pin : INTG# , INT#H  
 Request Indicate : REQ1#  
 Grant Indicate : GNT1#

# MINI-PCI

03/22 Add Diode to avoid EC keep RF\_EN Low.



# USB

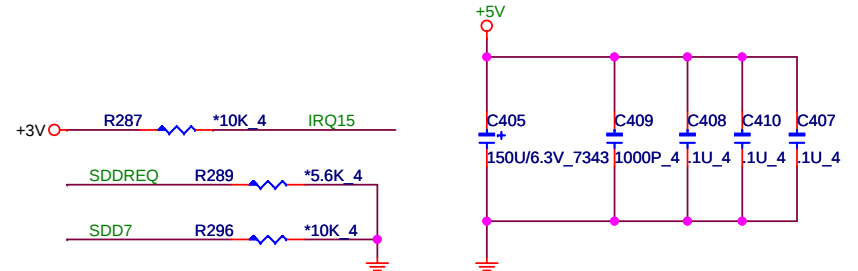
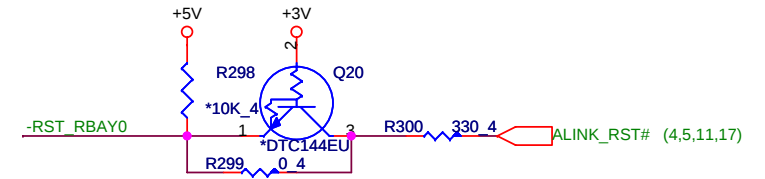
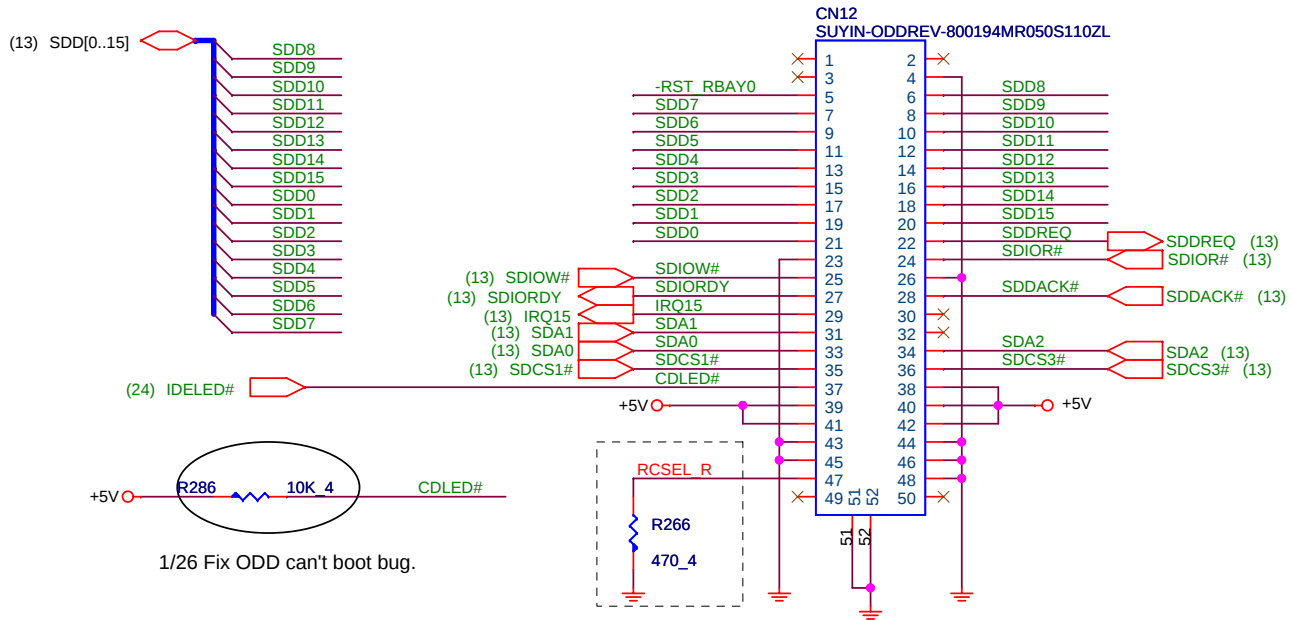


MPC

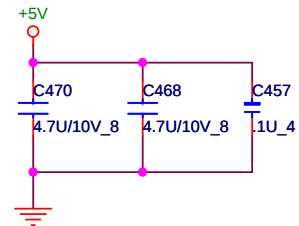
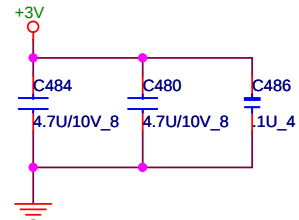
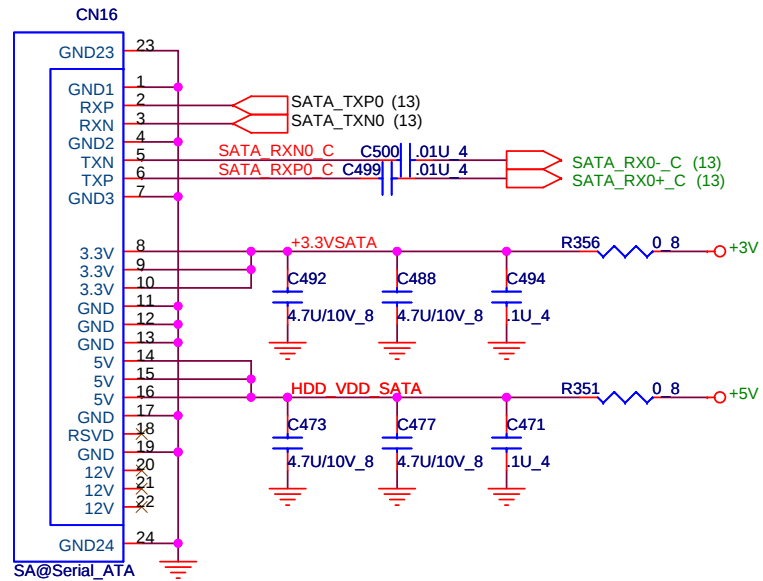
**PROJECT : BL1**  
**Quanta Computer Inc.**

|       |                       |                |
|-------|-----------------------|----------------|
| Size  | Document Number       | Rev            |
|       | <b>MINI PCI,USB</b>   | <b>3B</b>      |
| Date: | Tuesday, May 09, 2006 | Sheet 17 of 30 |

## ODD CONN



**SATA HDD CONN**



# IDE

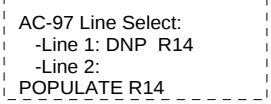


**PROJECT : BL1**  
**Quanta Computer Inc.**

|       |                                           |                |
|-------|-------------------------------------------|----------------|
| Size  | Document Number<br><b>HDD &amp; CDROM</b> | Rev<br>2A      |
| Date: | Monday, May 08, 2006                      | Sheet 18 of 30 |

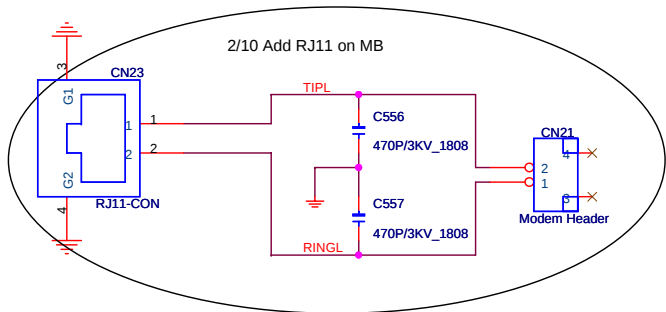




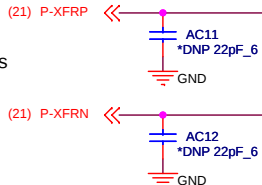


Title **DELPHI SV92A3 MDC 1.5 Reference Design**

Agere Systems Proprietary  
DRAFT COPY - FOR REVIEW ONLY  
SUBJECT TO CHANGE



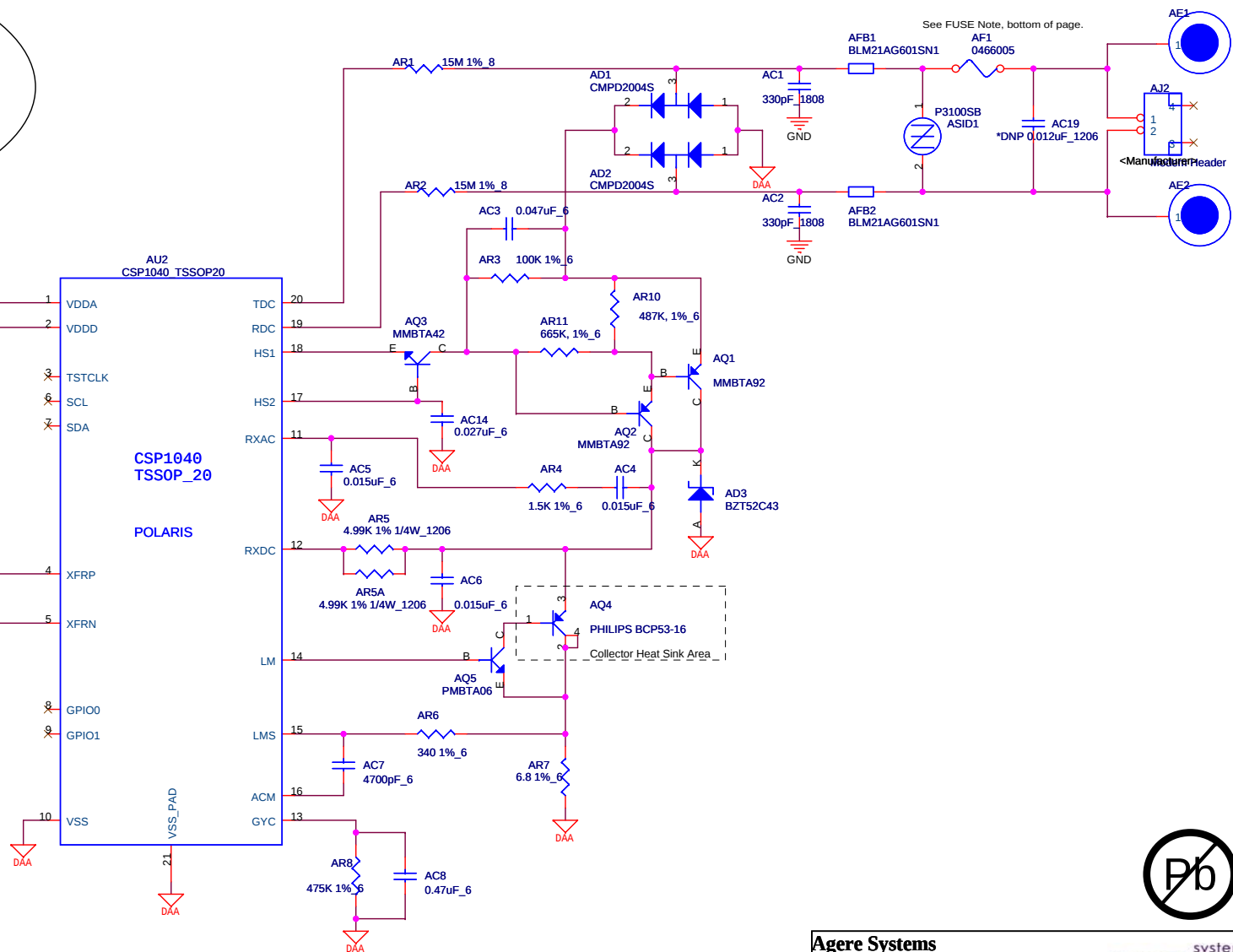
Locate C11, C12 as close to digital device as possible.



# MDM

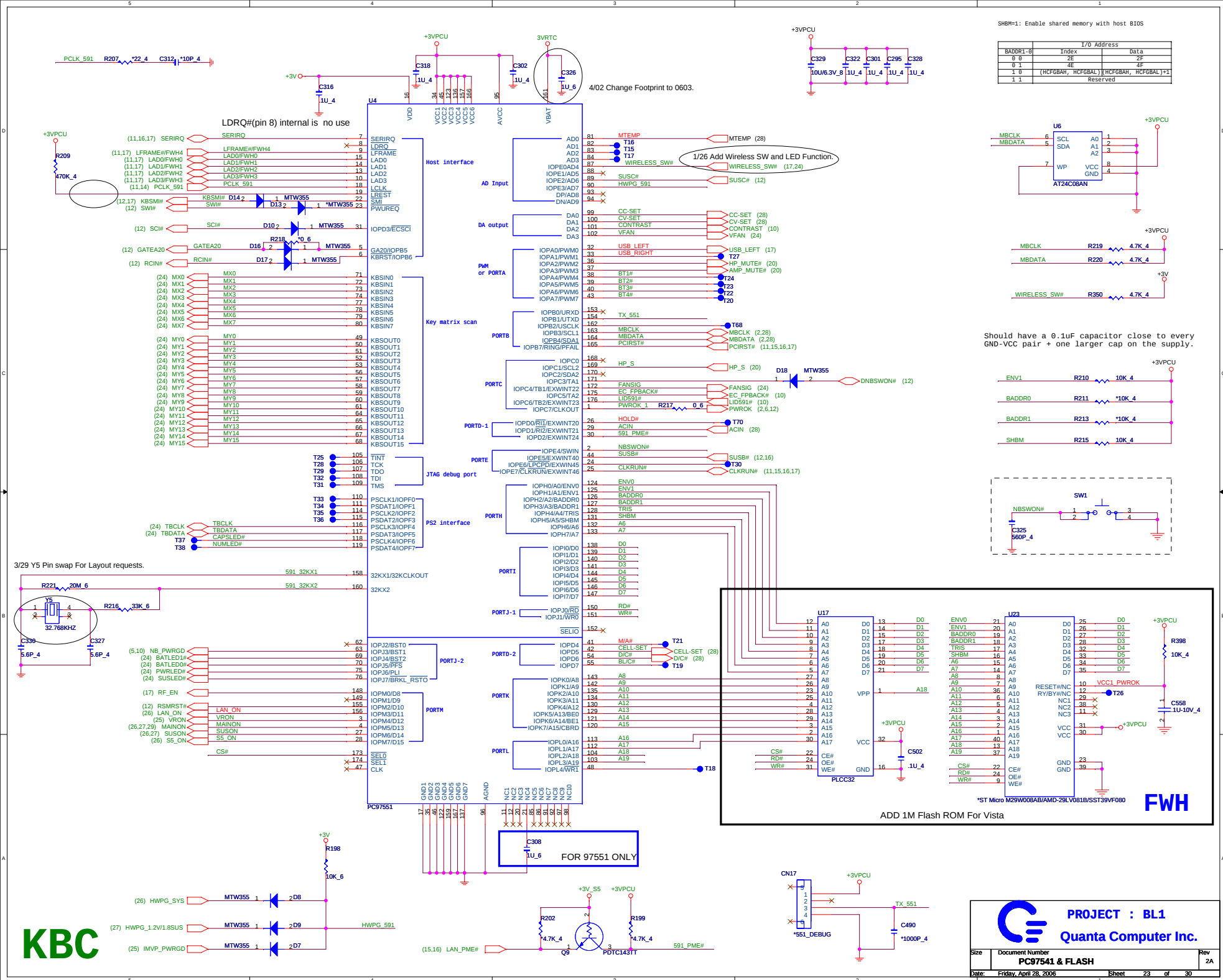
**FUSE Note:**  
The UL standard UL 1950 dictates the use of a fuse (needed to pass the M1, 600 V, 40A, 1.5 sec) to prevent component flaming during the overvoltage test. Unless one can insure that the modem is in a fire enclosure and provide 26 gauge line cord (acts as a fuse), a fusing element would be required.

Alternatively, if a TNV-1 flame resistant material is used, either as a wrap or cover over the DAA portion of the modem, this could satisfy both overvoltage protection and the separation requirement also contained in UL 1950. This latter requirement provides isolation such that unearthed parts of the DAA cannot be touched by a test finger or test probe.

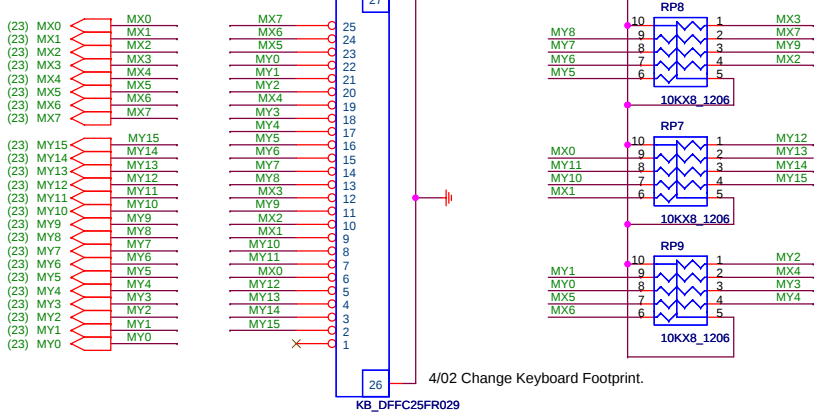


|                                               |                                       |           |
|-----------------------------------------------|---------------------------------------|-----------|
| <b>Agere Systems</b><br>Holmdel NJ            |                                       |           |
| <b>Design Engineer: R. Trevino</b>            |                                       |           |
| <b>DELPHI SV92A3 MDC 1.5 Reference Design</b> |                                       |           |
| Size B                                        | Document Number<br><b>CSP1040 DAA</b> | Rev<br>2A |
| Date: Saturday, May 06, 2006                  | Sheet 22 of 30                        |           |

Agere Systems Proprietary  
DRAFT COPY - FOR REVIEW ONLY  
SUBJECT TO CHANGE



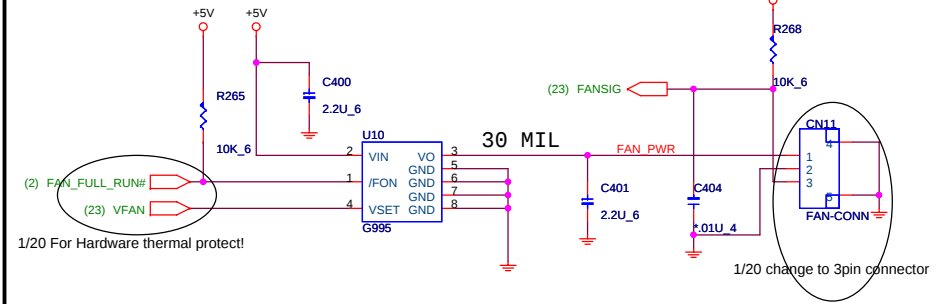
INT K/B



KBC

THM

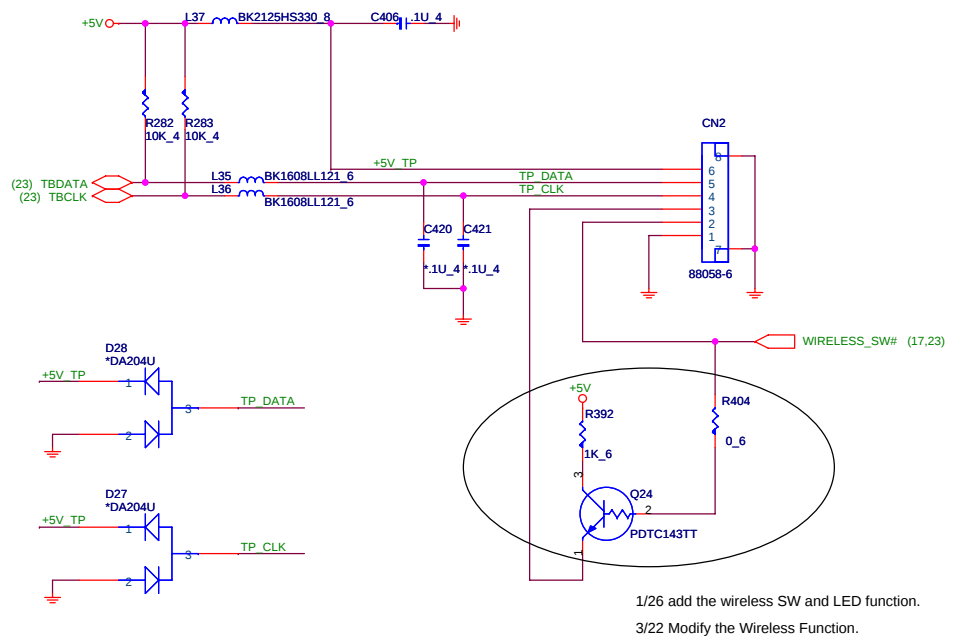
FAN CONTROL



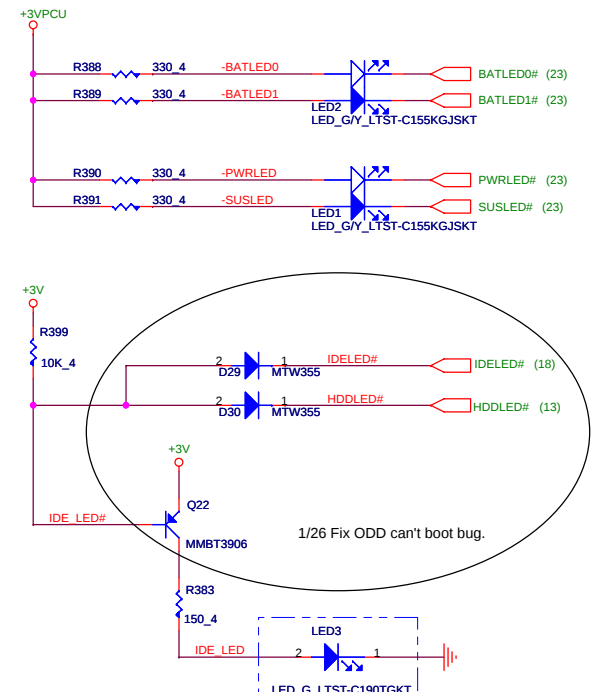
ON BOARD LED

TOUCH PAD

20 MIL



TPD



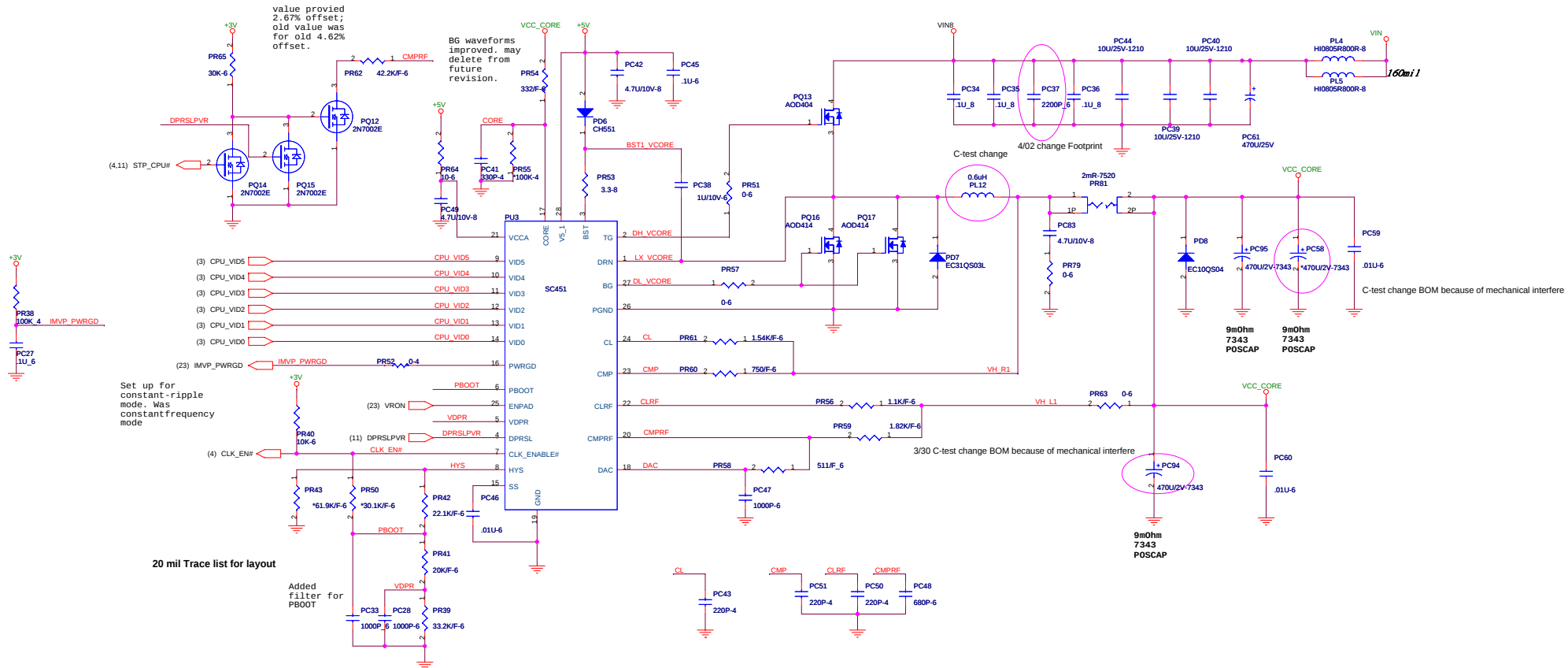
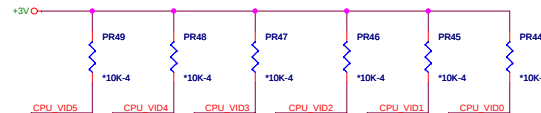
DCD

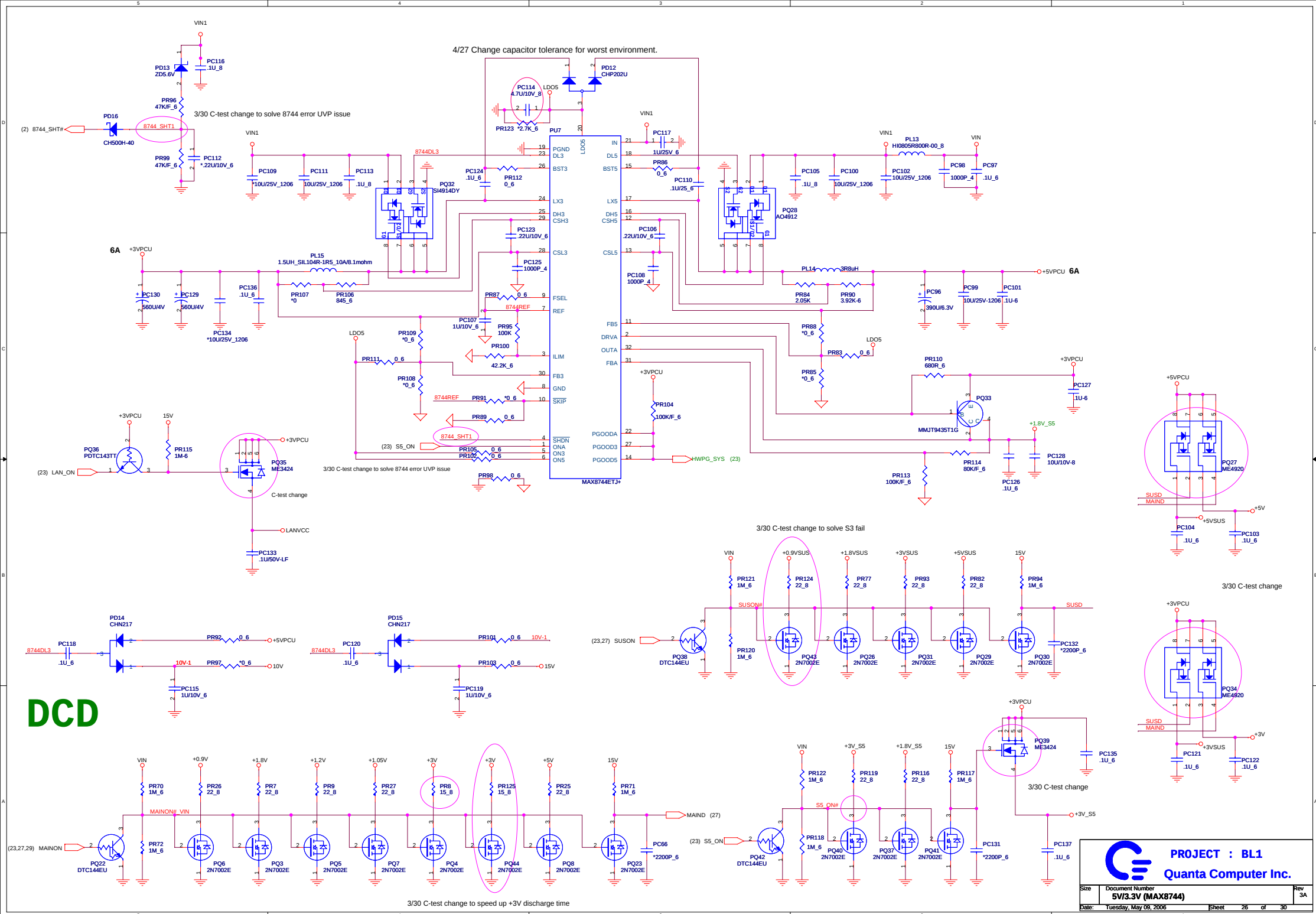
| V I D |       |       |       |       |       |       |  | Vcore |
|-------|-------|-------|-------|-------|-------|-------|--|-------|
| VID 5 | VID 4 | VID 3 | VID 2 | VID 1 | VID 0 | V     |  |       |
| 0     | 1     | 0     | 1     | 1     | 1     | 1.340 |  |       |
| 0     | 1     | 1     | 0     | 0     | 0     | 1.324 |  |       |
| 0     | 1     | 1     | 0     | 1     | 0     | 1.292 |  |       |
| 0     | 1     | 1     | 1     | 0     | 0     | 1.260 |  |       |
| 0     | 1     | 1     | 1     | 1     | 0     | 1.244 |  |       |
| 0     | 1     | 1     | 1     | 1     | 1     | 1.212 |  |       |
| 1     | 0     | 0     | 0     | 0     | 1     | 1.180 |  |       |
| 1     | 0     | 0     | 0     | 1     | 1     | 1.148 |  |       |
| 1     | 0     | 0     | 1     | 1     | 0     | 1.100 |  |       |
| 1     | 0     | 1     | 0     | 0     | 1     | 1.052 |  |       |
| 1     | 0     | 1     | 0     | 1     | 1     | 1.020 |  |       |
| 1     | 0     | 1     | 1     | 1     | 0     | 0.972 |  |       |
| 1     | 1     | 0     | 0     | 0     | 0     | 0.940 |  |       |

100 mil Trace list for layout

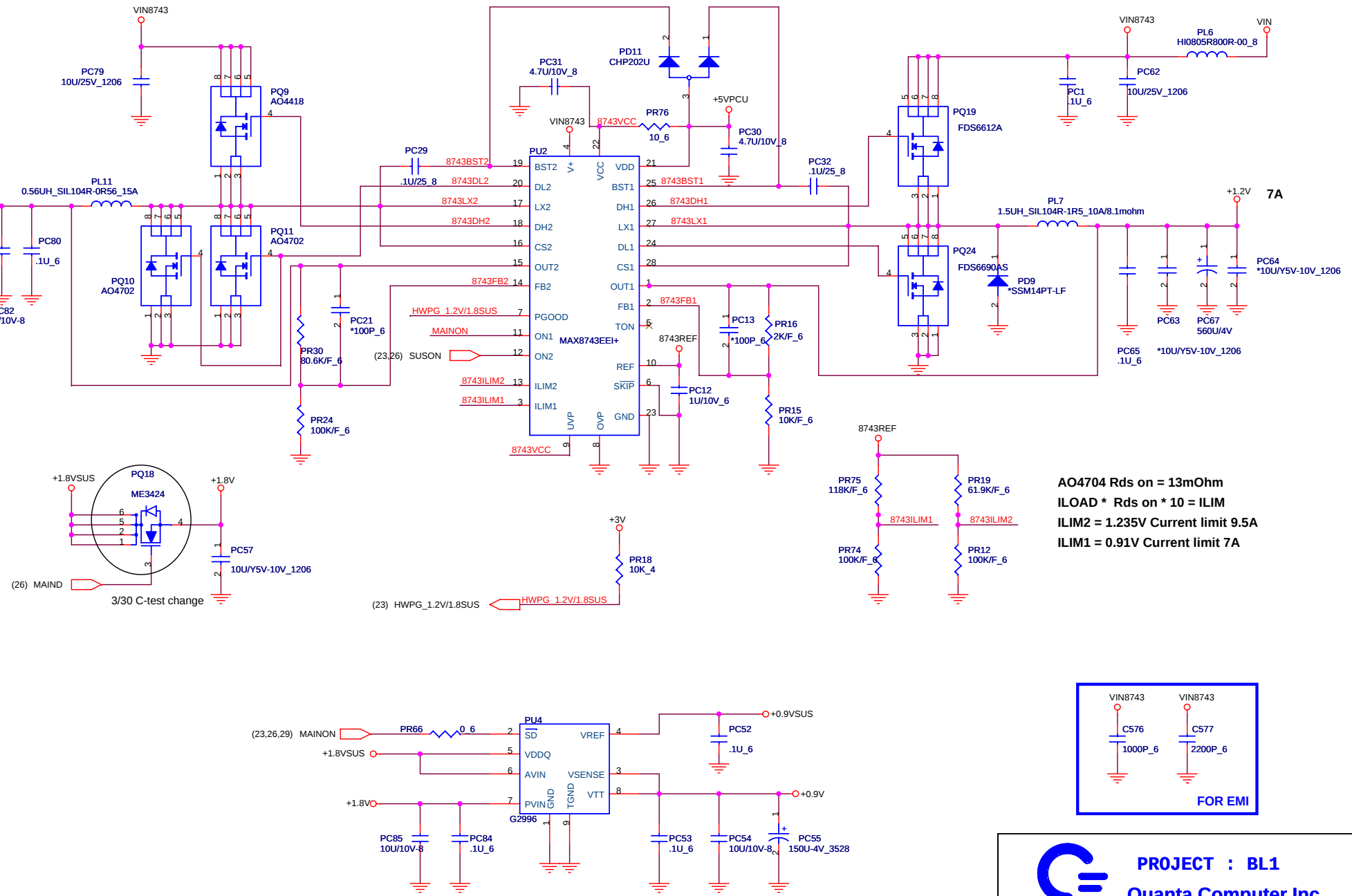
DH\_VCORE  
LX\_VCORE  
DL\_VCORE  
DH\_VCORE2  
LX\_VCORE2  
DL\_VCORE2

10 mil Trace list for layout  
SC1476  
pin 4 pin  
5 pin 7  
pin 25  
pin 30

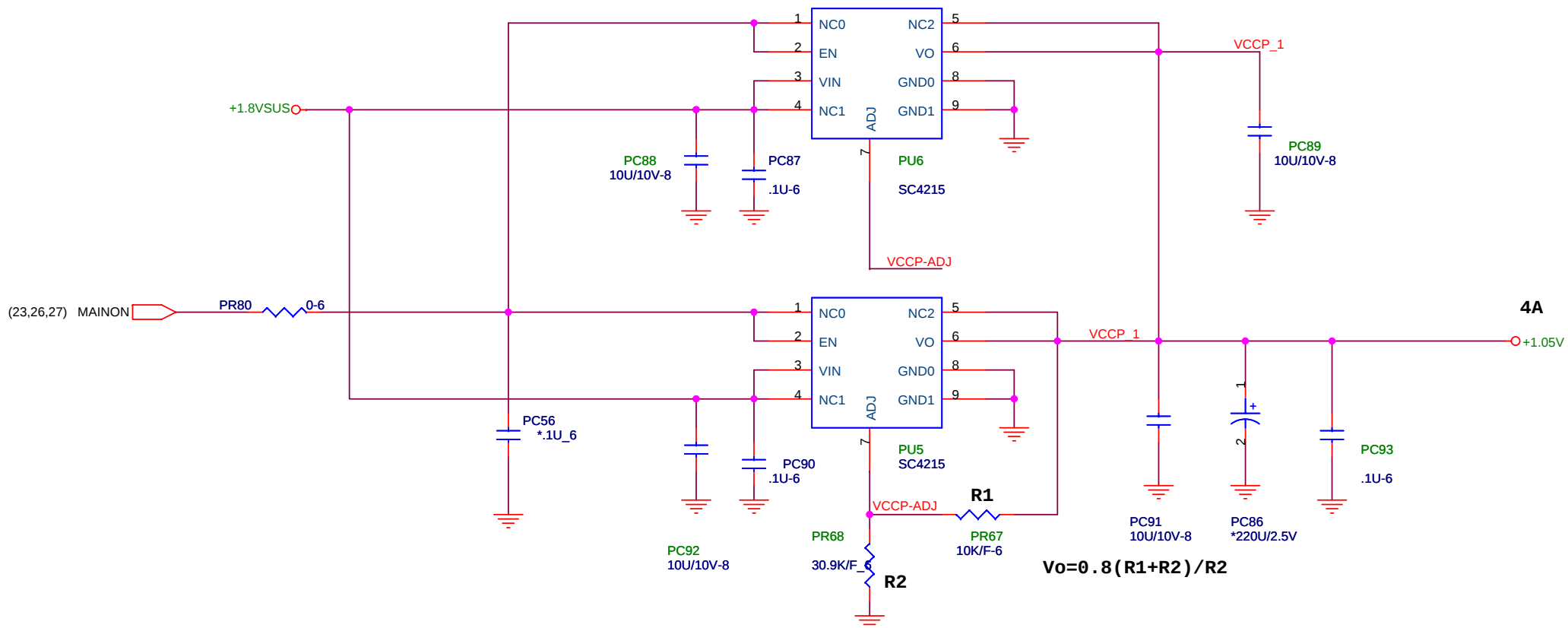




# DCD







DCD



PROJECT : BL1  
Quanta Computer Inc.

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